WHAT IS CLAIMED IS:

1. A semiconductor element comprising:

a source and a drain;

a first gate for forming a channel region of a uniform electric field between said source and said drain; and

a second gate for forming a channel region of a nonuniform electric field formed of strong and weak electric field regions, wherein

said first and second gates are located between said source and said drain, and overlap at least partially each other in a plan view, and

a conductance of the whole channel region between said source and said drain changes as a conductance of said channel region provided by said second gate changes in accordance with a voltage applied to said second gate.

2. The semiconductor element according to claim 1, wherein

occurrence of said strong electric field region and said weak electric field region partially changes a direction of the electric field in the whole channel region formed by said first and second gates, and said change in electric field direction modulates the effective gate length and gate width in said whole channel region.

3. The semiconductor element according to claim 1, wherein

said first gate has a rectangular form, and

said second gate has a geometry defined by a group of straight lines extending along the geometry of said first gate.

4. The semiconductor element according to claim 1, wherein

a conductance of a whole channel region including channels formed response by said first and second gates is controlled in accordance with voltages applied to said first and second gates.

5. The semiconductor element according to claim 1, wherein

an electric field vector in a whole channel region formed by said first and second gates is modulated in accordance with a ratio between voltages applied to said first and second gates, respectively.

6. The semiconductor element according to claim 1, wherein said first and second gates are layered with an insulating layer interposed between said first and second gates for electrical isolation.

7. The semiconductor element according to claim 1, wherein geometry of said first and second gates are designed such that the channel regions respectively formed by said first and second gates between said source and said drain have geometrical continuity.

8. The semiconductor element according to claim 1, wherein in the region between said source and said drain, a first portion overlapping with said first gate in a plan view has an impurity concentration different from that of a second portion not including said first portion but overlapping with said second gate in a plan view.

9. The semiconductor element according to claim 1, wherein in the region between said source and said drain, a first portion overlapping with said first gate in a plan view has an impurity concentration substantially equal to that of a second portion not including said first portion and overlapping with said second gate in a plan view.

10. A semiconductor element comprising:

a source and a drain;

a first gate having a rectangular form for forming a channel region between said source and said drain; and

a second gate for forming a channel region between said source and said drain, geometry of said second gate being defined by a group of straight lines along the geometry of said first gate, and having a gate length partially variable depending on a position along the gate width,

wherein

said second gate is formed in a region between said source and said drain, and overlaps at least partially with said first gate in a plan view.

11. The semiconductor element according to claim 10, wherein said second gate in the region between said source and said drain covers said first gate in a plan view.

12. The semiconductor element according to claim 10, wherein said second gate is configured to leave a portion not provided with said second gate within a region overlapping with said first gate in a plan view.

13. The semiconductor element according to claim 12, wherein said second gate is not formed in a central portion, in a direction of a gate width, within the region overlapping with said first gate in a plan view, and is formed in a portion other than the central portion.

14. The semiconductor element according to claim 12, wherein said second gate is formed in a central portion, in a direction of a gate width, within the region overlapping with said first gate in a plan view, and is not formed in a portion other than the central portion.

15. The semiconductor element according to claim 10, wherein a conductance of a whole channel region including channels formed response by said first and second gates is controlled in accordance with voltages applied to said first and second gates.

16. The semiconductor element according to claim 10, wherein an electric field vector in a whole channel region formed by said first and second gates is modulated in accordance with a ratio between voltages applied to said first and second gates, respectively.

17. The semiconductor element according to claim 10, wherein said first and second gates are layered with an insulating layer interposed between said first and second gates for electrical isolation.

18. The semiconductor element according to claim 10, wherein geometry of said first and second gates are designed such that the channel regions respectively formed by said first and second gates between said source and said drain have geometrical continuity.

19. The semiconductor element according to claim 10, wherein in the region between said source and said drain, a first portion overlapping with said first gate in a plan view has an impurity concentration different from that of a second portion not including said first portion but overlapping with said second gate in a plan view.

20. The semiconductor element according to claim 10, wherein in the region between said source and said drain, a first portion overlapping with said first gate in a plan view has an impurity concentration substantially equal to that of a second portion not including said first portion and overlapping with said second gate in a plan view.

21. A logic circuit comprising:

first and second field-effect transistors connected in series between nodes respectively supplying first and second voltages, and having a first conductivity type and a conductivity type opposite to said first conductivity type, respectively;

each of said first and second field-effect transistors including:

a source and a drain,

a rectangular first gate for forming a channel region between said source and said drain, and

a second gate formed in a region between said source and said drain for forming a channel region between said source and said drain, and overlapping at least partially with said first gate in a plan view;

geometry of said second gate being defined by a group of straight lines along geometry of said first gate, and providing a gate length discontinuously changing at least in one position along the gate length;

a signal input node connected to said first gate of each of said first and second field-effect transistors;

a signal output node connected to connection nodes of said first and second field-effect transistors; and

a control input node for controlling voltages applied to said second gates of said first and second field-effect transistors.

22. The semiconductor element according to claim 21, wherein said control input node applies a common voltage to said second gates of said first and second field-effect transistors.

23. The semiconductor element according to claim 21, wherein said control input node applies independent voltages to said second gates of said first and second field-effect transistors, respectively.

24. A logic circuit comprising:

first and second field-effect transistors connected in series between nodes respectively supplying first and second voltages, and having a first conductivity type and a conductivity type opposite to said first conductivity type, respectively;

each of said first and second field-effect transistors including:

a source and a drain,

a rectangular first gate for forming a channel region between said source and said drain, and

a second gate for forming a channel region between said source and said drain, geometry of said second gate being defined by a group of straight lines along the geometry of said first gate, and having a gate length partially variable depending on a position along the gate width,

said second gate being formed in a region between said source and said drain, and overlapping at least partially with said first gate in a plan

view;

a signal input node connected to said first gate of each of said first and second field-effect transistors;

a signal output node connected to connection nodes of said first and second field-effect transistors; and

a control input node for controlling voltages applied to said second gates of said first and second field-effect transistors.

25. The semiconductor element according to claim 24, wherein said control input node applies a common voltage to said second gates of said first and second field-effect transistors.

26. The semiconductor element according to claim 24, wherein said control input node applies different voltages to said second gates of said first and second field-effect transistors, respectively.